REMARKS

Claims 8-12 and 14-16 are pending. Claims 8-12 and 14-15 have been withdrawn as being directed to a non-elected invention.

The Office Action rejects claim 16 under 35 U.S.C. 102(b) as being anticipated by Jacobs et al. (U.S. Patent No. 4,027,320). This rejection is traversed.

The semiconductor according to the present claim is formed by adjusting the threshold voltage so as to be substantially equal to that of a normal MOS transistor without Kr. In the presently claimed invention, without using a thermal oxide conventional film, a good characteristic of threshold voltage is obtained using Kr/O_2 plasma (see Figures 14 and 15 of the present application).

Kr/O_2 plasma enables insulating film formation at low temperatures. As a result, the insulating film contains Kr, and the presence of Kr affects the threshold voltage.

Jacobs merely teaches that an insulating film contains Kr.

If a normal MOS transistor containing Kr is formed with no regard to the above condition, the threshold voltage would be different from that of a normal MOS transistor without Kr, due to the differences in methods.

In particular, any procedure that affects any of the parameters that make up the threshold voltage will, of course, correspondingly affect the threshold voltage. Thus, for example, changing the trap density would be expected to affect the threshold voltage.

For example, Applicants have attached hereto a copy of a paper titled "A Technology for Reducing Flicker Noise for ULSI Applications" by Tanaka et al. (Jpn. J. Appl. Phys. Vol. 42 (2003) pp 2106-2109). In this paper, it is demonstrates that, with

reference to Table 1 on page 2108, "conventional thermal oxidation makes the Si/SIO_2 interface roughness [while on] the other hand, radical oxidation using microwave-excited high-density Kr/O_2 plasma...corresponds to the bare silicon surface roughness after atomic scale flattening...This result indicates that radical oxidation using high-density Kr/O_2 plasma enables growth of oxide films without increasing the Si/SiO_2 interface roughness." (see the first paragraph on page 2108). The results in the paper demonstrate that "the atomic scale flattening process can effectively reduce the interface trap density" (see the first full sentence on the left side of page 2108).

Table 1 of the above-discussed paper clearly shows that the Kr/O2 plasma results in a lower subtheshold swing value and a lower interface trap density. Thus, treatment with Kr/O_2 clearly affects trap density and threshold value.

In Jacobs et al., "the lattice defect or trap density and the position of the lattice defects or traps in the gate insulation layer can be selected in optimal fashion by a predetermined setting of the implantation parameters (dose, depth of entrance, dopant)" (column 1, lines 61-65).

Thus, it is the advantage of Jacobs et al. to alter the trap density, which would be expected to alter the threshold voltage.

Thus, as the Jacobs et al. threshold voltage would be expected to be different after the implantation process, the threshold voltage would be different before any Krypton is added in comparison to after any Krypton is added.

It is therefore respectfully submitted that Jacobs et al. fails to teach or suggest the above-discussed condition required by the presently claimed invention, namely that the threshold voltage is substantially equal to that of a normal MOS transistor without

Kr. The threshold voltage of the MOS transistor of Jacobs et al. would have been expected to be different from that of a normal MOS transistor without Kr, unless a MOS transistor is made to realize the above-discussed condition required by the presently claimed invention.

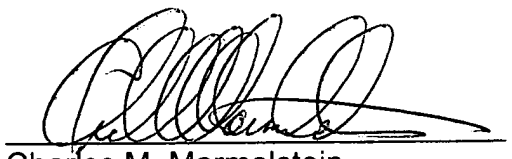
In view of the above, reconsideration and withdrawal of the rejection of claim 16 under 35 U.S.C. 102(b) are respectfully requested.

Applicant also takes this opportunity to submit herewith verified translations of the foreign priority documents that were relied upon for Applicant's priority claim.

In view of the above remarks and amendments, Applicant respectfully submits that all of the pending claims are in condition for allowance. Favorable consideration and prompt allowance of the claims and this application are earnestly solicited. Should the Examiner believe anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's representatives at the telephone number listed below.

In the event this paper is not considered to be timely filed, Applicant respectfully petitions for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees that may be required with respect to this paper or credit any overpayment to Counsel's Deposit Account 01-2300, making reference to Attorney Docket No. 108390-00056.

Respectfully submitted,



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Enclosures: Tanaka et al., "A Technology for Reducing Flicker Noise for ULSI Applications"
Petition for Extension of Time (two months)

Jpn. J. Appl. Phys. Vol. 42 (2003) pp. 2106–2109
Part 1, No. 4B, April 2003

A Technology for Reducing Flicker Noise for ULSI Applications

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It is demonstrated that the formation of the atomic scale flattened Si/SiO_2 interface is effective in reducing the Flicker noise in n-channel metal oxide semiconductor field effect transistors (n-MOSFETs). The atomic scale flattened Si/SiO_2 interface is realized, the atomic scale flattened silicon surface is obtained by the HF/HCl wet-etching process, and then the silicon surface is oxidized by radicals generated in Kr/O_2 mixed high-density microwave-excited plasma at 400 °C. Applying these techniques, the trap density at the Si/SiO_2 interface is markedly reduced since the surface roughness is minimized and Flicker noise is markedly reduced as compared with the conventional process. [DOI: 10.1143/JJAP.42.2106]

KEYWORDS: flicker noise, high-density plasma, radical oxidation, surface roughness, atomic scale flattening, AFM, STM

1. Introduction

Miniaturization of metal oxide semiconductor field effect transistors (MOSFETs) realizes high integration and high-speed performance of ULSI devices. The bias voltage (V_{DD}) also must be reduced to realize systems with low power consumption. However, it is a concern that the signal to noise (SN) ratio degenerates since the small signals are buried in noise, which may be thermal noise or/and Flicker noise. Particularly, Flicker noise is very important for ultra LSI (ULSI) applications at analog fields since its power density increases if the scaling is progressing.[1,2] For future ULSI technologies, a very low Flicker noise device requires an essential technology.

Flicker noise is, in general, caused by fluctuation of the number of carriers in an inversion layer as they are captured and emitted from traps located at the Si/SiO_2 interface and oxide in the gate.[3] Consequently, reducing the traps at Si/SiO_2 interface is very essential in developing very low Flicker noise devices.

In this study, n-channel MOSFETs (n-MOSFETs) were fabricated on flattened[4,5] and conventional silicon substrates, and the radical oxidation technology is applied to gate oxidation to control the interface traps. Finally, the Flicker noise power spectrum density (PSD) was compared between the n-MOSFET on the atomic scale flattened substrate and that on the conventional substrate. These technologies can reduce the PSD of Flicker noise compared with the conventional technology.

2. Experimental

n-MOSFETs were fabricated on two types of silicon wafers, which of the Cz p-type [0.09–0.2 Ω-cm]. One type was oriented exactly (100) surface and the other was oriented 4°-off [010] on the (100) surface (4°-off substrate). Figure 1 shows the 4°-off [010] substrate on the (100) surface.

A 400 nm-thick SiO_2 film (field oxide) was grown on each wafer (conventional wet oxidation at 1,000°C). A field oxide film, which was grown on 4°-off wafer, was etched until it was 30 nm thick at the active region by wet etching. The remaining field oxide film was etched with a very low pH (<1) solution (HF(50%):HCl(37%)=1:19) to formulation atomic scale step layer on the silicon surface after modified (RCA) cleaning.[6] Finally, an atomic scale flattened substrate was obtained. On the other hand, the field oxide film of the conventional (100) surface wafer was etched with conventional etching solution. Figure 2 shows the process flow for the 4°-off wafer and conventional wafer.

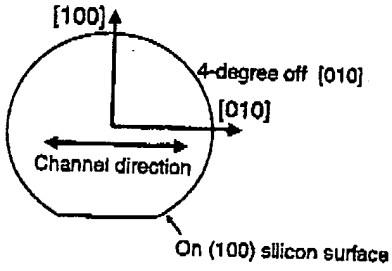

Fig. 1. 4 -off [010] substrate on (100) surface.

We applied the scanning tunneling microscopy (STM) to observe the nanoscopic surface. Figures 3(a) and 3(b) show

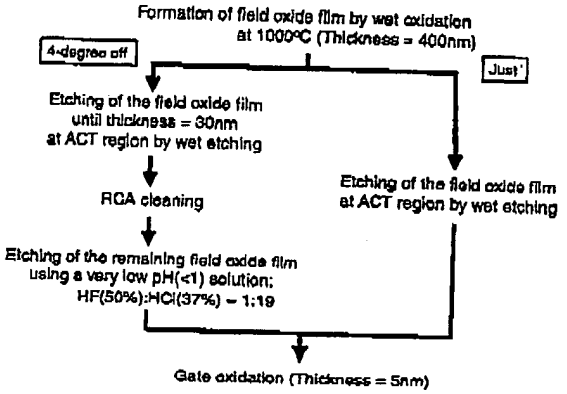

Fig. 2. Wet-process flow.

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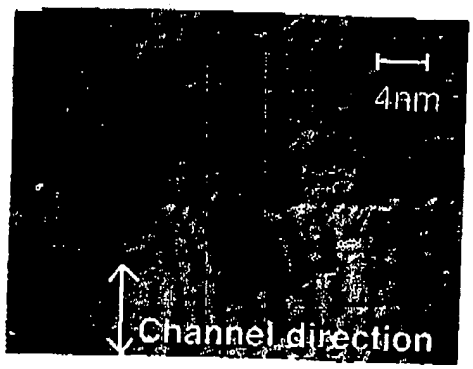
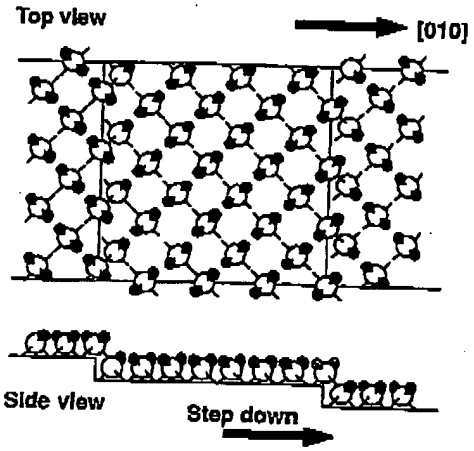


(a)



(b)

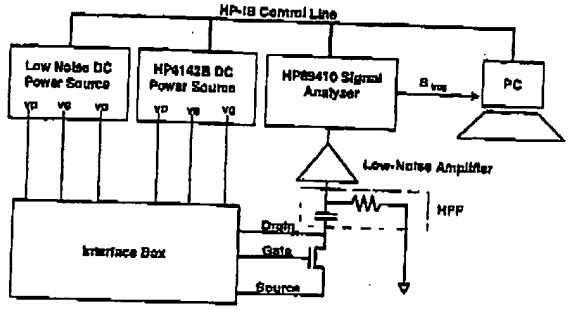
Fig. 3. (a) STM image of 4°-off substrate on (100) surface. (b) Illustrated STM image of 4°-off substrate on (100) surface.

the STM image of the flattened surface and the illustrated STM image, respectively. We also used the atomic force microscopy (AFM) to measure the average surface roughness (R_a) at the Si/SiO_2 interface. Gate oxide films (5 nm-thick) were grown by the conventional thermal oxidation at 900°C and radical oxidation using microwave-excited high-density Kr/O_2 plasma at 400°C.[6] The 500 nm- thick n^+ poly-silicon gate electrodes were formed by chemical vapor deposition (CVD). The subsequent steps were the source/drain formation, the conventional passivation, the contact opening, the metallization, and the H_2/N_2 sintering at 400°C.

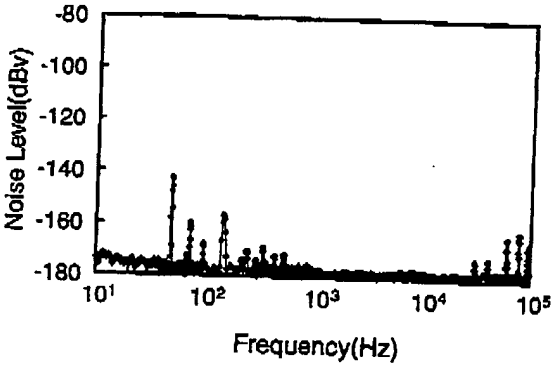
Figures 4(a) and 4(b) show the Flicker noise measurement system and its noise level, respectively. On wafer 1/f noise was measured over the frequency range of 10 Hz to 100 kHz using an HP89410 signal analyzer in conjunction with a low-noise preamplifier. The DC bias for the device tested was supplied by the ShibaSoku PA14A1 via the Agilent Technology Interface Box, resulting in a system noise level of below −175 dBv.

3. Results and Discussions

Figure 5 shows the R_a values for three samples, which are bare silicon after modified RCA cleaning (Sample A), the oxide film grown in 100% O_2 at 900°C (Sample B), and the



(a)



(b)

Fig. 4. (a) Noise measurement system. (b) Noise level of system.

oxide film grown using Kr/O_2 plasma at 400°C (Sample C). After removal of the gate oxide film using HF(50%):HCl(37%)=1:19 solution, the R_a values were measured by the AFM. The R_a value for sample A on the 4°-off substrate is lower than that on the substrate of the (100) surface. This result indicates that the removal of the oxide film grown on the 4°-off wafer using HF(50%):HCl(37%)=1:19 solution is effective for realizing an atomic scale flat on silicon surface. The R_a value (0.2 nm) for the oxide film grown on the 4°-off substrate sample B is

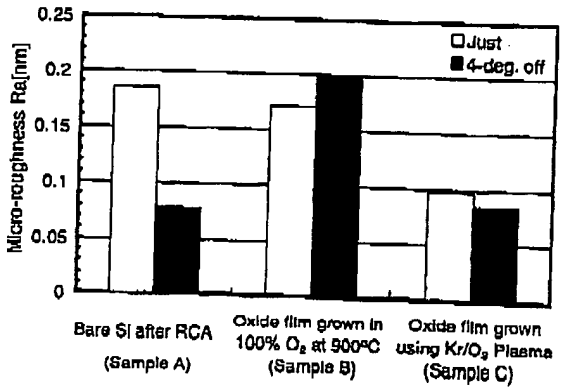


Fig. 5. Measured surface roughness of bare silicon after modified RCA and Si/SiO_2 interface.

Table I. Subthreshold swing value and interface trap density.

	Dry 900°C	Dry 900°C Flat	Kr/O_2 Flat
Subthreshold swing value [mV/dec]	75	71	68
Interface trap Density [c/cm^2]	4.34×10^{11}	6.88×10^{10}	3.13×10^{10}

higher than the bare silicon R_a value. It means that the conventional thermal oxidation makes the Si/SiO_2 interface roughness. On the other hand, radical oxidation using microwave-excited high-density Kr/O_2 plasma, which is formed at 400°C, corresponds to the bare silicon surface roughness after atomic scale flattening, and the R_a value is 0.08 nm. This result indicates that radical oxidation using microwave-excited high-density Kr/O_2 plasma enables growth of oxide films without increasing the Si/SiO_2 interface roughness.

Table I shows the subthreshold swing values and the interface trap density. The subthreshold swing values and interface trap density for two types of MOSFET (one type is oxidized by the conventional thermal oxidation at 900°C, the other type is oxidized by Kr/O_2 radical at 400°C) including the atomic scale flattening process are lower than those not including the atomic scale flattening process. These results indicate that the atomic scale flattening process can effectively reduce the interface trap density.

Figure 6(a) shows the PSD of Flicker noise in two types of n-MOSFET at a drain-source voltage (V_{DS}) of 1.5 V, and a gate-overdrive voltage (V_{GT}) of 1.5 V. The Flicker noise PSD in n-MOSFETs fabricated by the thermal oxidation process including the atomic scale flattening process is one order of magnitude lower than that in n-MOSFETs fabricated on a conventional substrate in the intermediate region. This result indicates that the thermal oxidation process including the atomic scale flattening process is very effective in reducing Flicker noise. However, the thermal oxidation process including the atomic scale flattening process does not markedly reduce Flicker noise in the saturation region (Fig. 6(b)).

Figure 7(a) shows the comparison of Flicker noise PSD between the radical oxidation process and the thermal

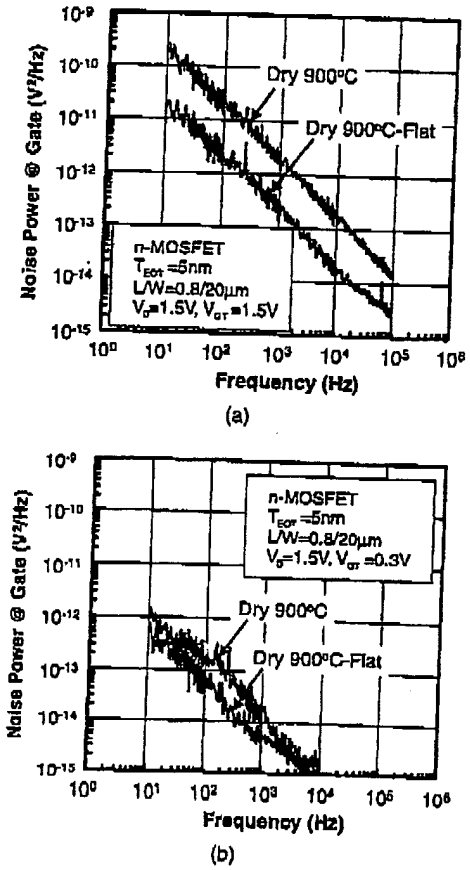


Fig. 6. (a) PSD of Flicker noise in intermediate region. (b) PSD of Flicker noise in saturation region.

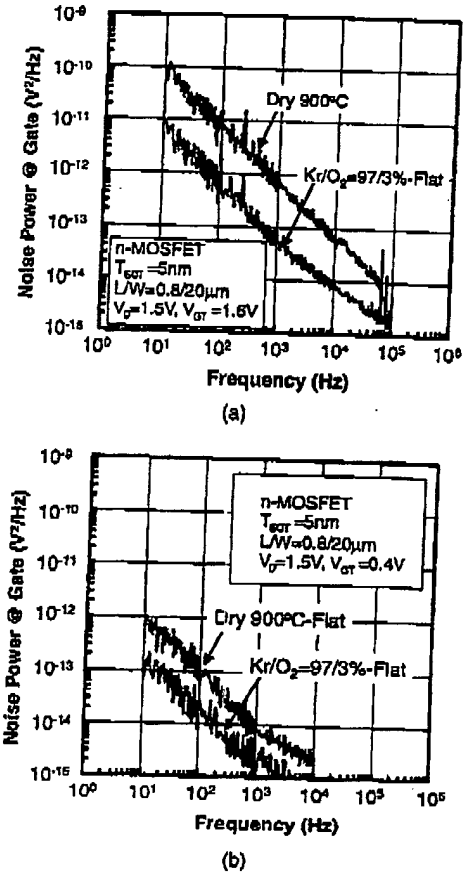


Fig. 7. (a) PSD of Flicker noise in n-MOSFET fabricated by Kr/O_2 radical oxidation including the atomic scale flattening process in intermediate region. (b) PSD of Flicker noise in n-MOSFET fabricated by Kr/O_2 radical oxidation including the atomic scale flattening process in saturation region.

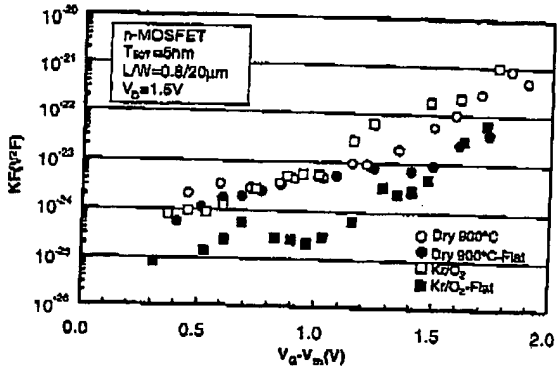


Fig. 8. Flicker noise coefficient (KF) vs. gate overdrive voltage (V_{GT}) characteristics.

oxidation process including the atomic scale flattening process at $V_{DS} = 1.5$ V and $V_{GT} = 1.6$ V. The Flicker noise PSD in the radical oxidation process is one order of magnitude lower than that in the conventional thermal oxidation process. Also, the radical oxidation process including the atomic scale flattening process is very effective in reducing Flicker noise in the saturation region (Fig. 7(b)).

Figure 8 shows gate-overdrive voltage - Flicker noise coefficient (V_{GT}–KF) characteristics for four types of n-MOSFET, which were obtained by dry oxidation at 900°C, dry oxidation including the atomic scale flatting process, radical oxidation, and radical oxidation including the atomic scale flatting process at $V_{DS} = 1.5$ V. This result indicates that the radical oxidation process including the atomic scale flattening process is very effective in reducting of Flicker noise in a wide range of V_{GT}.

These results indicate that the interface traps are markedly reduced when the atomic scale flattening and radical oxidation processes are applied. Consequently, Flicker noise is also markedly reduced.

4. Conclusion

The atomic scale flattened silicon surface can be obtained by treatment of the 4°-off silicon (100) surface with HF(50%):HCl(37%)=1:19 solution. Additionally, by applying the atomic scale flattening process and radical oxidation using microwave-excited high-density plasma, The Flicker noise can be markedly reduced. The Flicker noise PSD of n-MOSFETs obtained using these techniques is one order of magnitude lower than that obtained using the conventional process. Decrease in the SN ratio accompanying scaling can be minimized, and the reliability of ULSI devices can be improved using these technologies.

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